Comparative Study on the Impact of TiN and Mo Metal Gates on MOCVD-Grown HfO_2 and ZrO_2 High-κ Dielectrics for CMOS Technology

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Introduction

The reduction of the equivalent oxide thickness (EOT) of the gate oxide has emerged as one of the most difficult tasks addressing future CMOS technology. In order to overcome gate tunneling, the introduction of so-called high-κ materials will be necessary [1]. Hafnium dioxide, HfO_2 [2], zirconium dioxide, ZrO_2 [3], and their silicates are assumed to be the most promising candidates to fulfil the crucial demands necessary for a successful integration of high-ķ dielectrics into CMOS devices.

Along with the introduction of high-κ dielectrics, metal gates are anticipated to be introduced [1] to circumvent polysilicon-gate depletion [4] and high gate-resistance. *Mid-gap-metal* and *dual-work-function gate technology* are the two main concepts addressing the implementation of metal gates. Whereas TiN is a promising candidate to be applied as mid-gap metal gate [5], Mo is a suitable candidate for a single-metal, tunable dual-work-function technology [6].

By this work, we present a comprehensive study on Mo- and TiN MOS capacitors, including MOCVD-deposited ZrO_2 or HfO_2 as gate isolator, and the impact of annealing on slow and fast interface traps.

Experimental

As substrates we used boron-doped (100)-silicon wafers with a resistivity of 0.04 – 2.0 Ωcm. The substrates were subjected to a modified RCA-clean and a finalizing HF-dip immediately prior to deposition. ZrO_2 and HfO_2 thin films were deposited by MOCVD in a horizontal hot-wall reactor equipped with a bubbler system. Post-deposition annealing (PDA) of the samples was done in forming gas atmosphere (FGA) at 650°C. Subsequently, ~100 nm thick gate metals – in which the gate metal patterning was done by a lift-off process – were deposited on the high-κ dielectrics without capping to complete metal-oxide-semiconductor (MOS) capacitors. Finally, post-metallization annealing (PMA) in FGA and in some cases additionally high temperature annealing (RTA) in N_2 atmosphere has been applied.

Capacitance-Voltage (C-V) and Current-Voltage (I-V) characterizations have been performed, prior and after to the different annealing steps to evaluate electrical characteristics, respectively. To eliminate any parasitic series resistance in accumulation, all C-V curves have been corrected [7], and consequently EOT and Flatband voltage V_{FB} were deduced from quasistatic C-V measurements.

Results

Results for HfO_2 or ZrO_2 as gate dielectric are in general similar and comparable to each other. They revealed that PMA in FGA is effective in annealing out interface traps located in the Si bandgap in all investigated devices. Additionally, oxide charges are neutralized, as can be concluded from a shift of V_{FB} to more positive values in the C-V characteristics. The leakage current slightly rises due to PMA and we suppose thermodynamical reactions within the dielectrics during the thermal treatment to be responsible for this behavior.

The RTA treated samples exhibit a clearly decreased oxide charge density, but also an increase of C_{oxide} in accumulation, as well as an undesirable high leakage current. We therefore assume a crystallization process of the gate oxide that takes place during RTA and changes the bulk characteristics. High resolution-Transmission electron microscopy (HR-TEM) measurements, which reveal interfacial SiO_2 that might form already during PDA, support this assumption.

Titanium-Nitride Gate

Figure 1 shows C-V and I-V (inset) measurements for various frequencies for a TiN/ZrO_2/p-Si capacitor after PMA at 450°C in FGA. Only a small hump around ~0.25 V due to interface traps in the silicon bandgap can be seen. Up to at least 450°C, this gate stack shows thermodynamical stability.

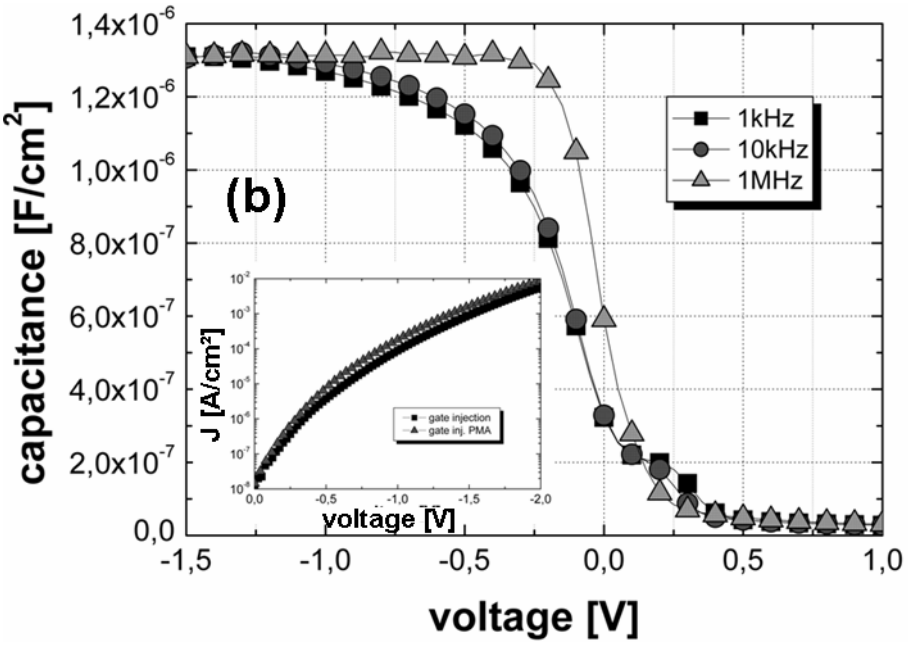

Fig. 1: C-V and I-V (inset) measurements of a TiN/ZrO_2/p-Si capacitor after PMA in FGA.

Molybdenum Gate

C-V and I-V (inset) measurements for various frequencies for a Mo/HfO_2/p-Si capacitor are shown in Fig. 2. Thermal treatment included PMA at 450°C in FGA and RTA at 950°C in N_2. A hump around ~0.0 V due to interface traps in the silicon bandgap can be seen. Leakage current after RTA is undesirably high, probably due to crystallization of the gate oxide during annealing.

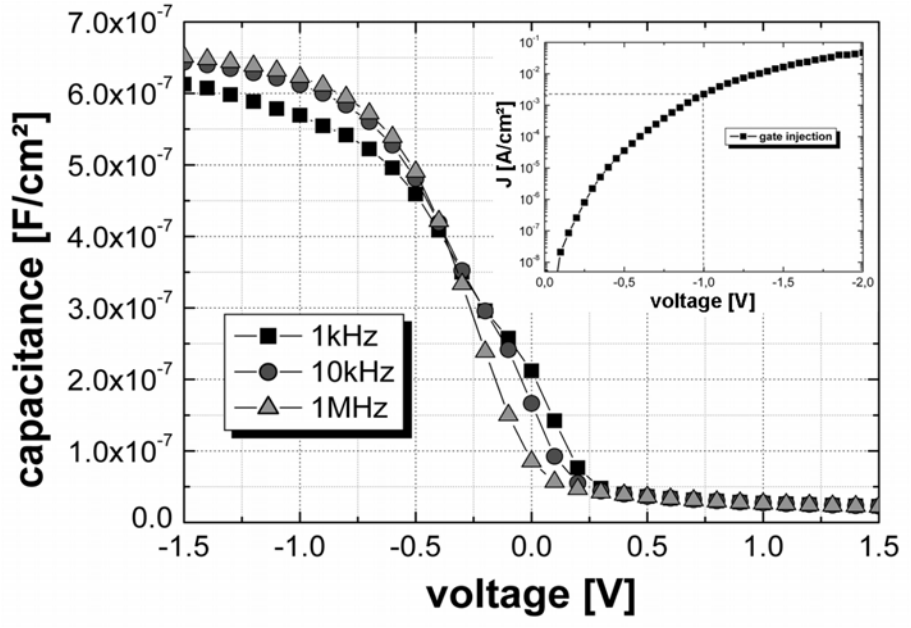

Fig. 2: C-V and I-V (inset) measurements of a Mo/HfO_2/p-Si capacitor after PMA in FGA and RTA in N_2.

Summary

A summary of the investigated gate stacks is shown in table 1. The V_{FB} values for the TiN- and Mo-capacitors indicate mid-gap pinning of the metal gates. One can see that the values of κ do not correlate with the corresponding EOT; a trade-off between EOT and κ is observed. This might be due to different contributions of an unintentional interfacial SiO_2 layer forming during the growth process and its further increase during post deposition annealing treatments.

Gate material:	TiN (PMA)	Mo (PMA+RTA)
EOT [nm]:	2.0	3.4
Diel. constant κ [1]:	12	23
Flatb. Volt. V_{FB} [V]	-0.05	-0.16
Ox. Dens. Q_0 [cm^{-2}]	1.1E+12	1.2E+10

Table 1: Summary of TiN- and Mo/ZrO_2/Si stacks.

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