Technology of InAlN/(In)GaN-Based HEMTs

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Introduction

InAlN/GaN-based HEMTs are excellent candidates for high power and high frequency applications, primarily because of the very high polarization-induced two-dimensional electron gas (n_{2DEG}) in the channel [1]. Therefore $In_xAl_{(1-x)}N$/(In)GaN performance is predicted to be superior in respect to AlGaN/GaN HEMTs. That allows obtaining higher drain saturation current and higher power. One of the most important factors that limits the performance and reliability of III-Nitride high electron mobility transistors (HEMTs) is a high gate leakage current. One way to overcome it is an introduction of an oxide layer under the gate contact. On the other hand AlGaN/GaN-based HEMTs are known to suffer from the trapping effects related to the surface states.

In this work we fabricate and investigate InAlN/GaN HEMTs with and without Al_2O_3 oxide under the gate.

Experimental

$In_xAl_{(1-x)}N$/AlN/GaN (x=0.17) heterostructures were grown by Metal Organic Chemical Vapor Deposition (MOCVD) on sapphire substrates. Free carrier concentration and mobility values of the 2D electron gas (2DEGs) were determined at room temperature by Hall measurements to be $3.0e^{13}$ cm^{-2} and 815 $cm^2V^{-1}s^{-1}$, respectively.

Standard photolithographic and lift-off techniques were used for processing the HEMT structure. Initially, the mesa region had been defined by reactive-ion etching (RIE) using a photoresist mask. $SiCl_4$ had been used as gas to etch 120 nm. The ohmic contact metallization [1] consisted of Ti/30 nm, Al/200 nm, Ni/40 nm, Au/50 nm. Just before deposition, samples were dipped into diluted HCl. Rapid thermal annealing (RTA) was performed in N_2 atmosphere for 120s at the annealing temperature. Various temperatures from 500 °C to 900 °C were tested and an optimized annealing temperature for device processing at 700 °C has been found. For the Schottky barrier contact we used Ni/30nm, Au/150 nm [1]. Prior to deposition the sample was etched in HF:HCl:H_2O 1:1:10 solution for 20 s. Furthermore, to reduce the leakage current, we are investigating the growth of Al_2O_3 and the performance of Al_2O_3/GaN MOS contacts. Al_2O_3 was grown in an AIXTRON triJet liquid precursor system at 600 °C using precursors of aluminium acetylacetonate dissolved in toluene. Various surface pre-treatments prior to

Al_2O_3 deposition will be discussed in terms of device performance. Al_2O_3 has been etched using Ar. The pressure and the V_{bias} were set at 15 mTorr and 300 V, respectively. Principal schemes of investigated structures are shown in Figure 1.

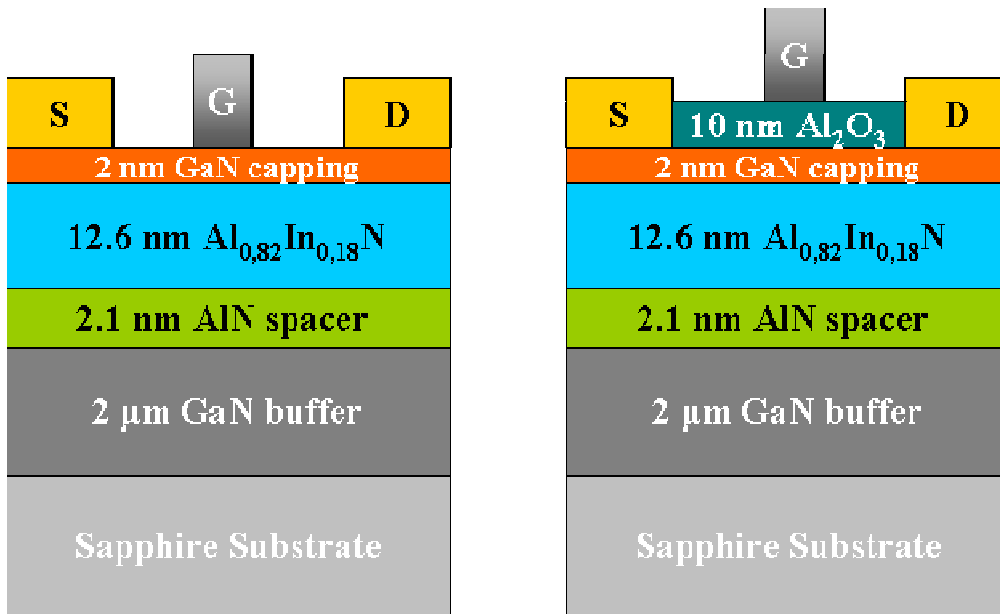

Fig. 1: Schematic cross section of GaN/InAlN/AlN/GaN with and without 10 nm AlO_2

Results

Significant leakage current reduction (2 orders of magnitude less) on MOS (Al_2O_3/Ar) was observed when compared with a reference Schottky barrier contact (Fig. 2). A comparable leakage current was found for MOS with different pre-treatment.

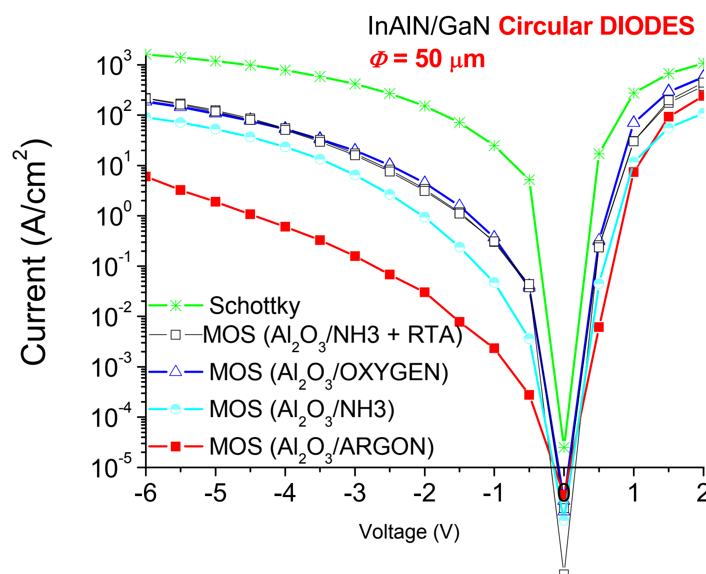

Fig. 2: Gate leakage current of MOS compared with the Schottky structure.

In Fig. 3 we show DC and Gate Lag (GL) pulsed (200 ns length) output characteristics of the InAlN/AlN/GaN HEMT. Clearly no Gate Lag effect can be seen. We assume that AlN insertion may decrease or even revert the electric field in the InAlN without affecting the n_{2DEG}. We prevent the potential energy from rising and thus our approach may eliminate surface state generation *during* InAlN growth. That may explain the reduction of the current collapse for InAlN/AlN/GaN HEMTs.

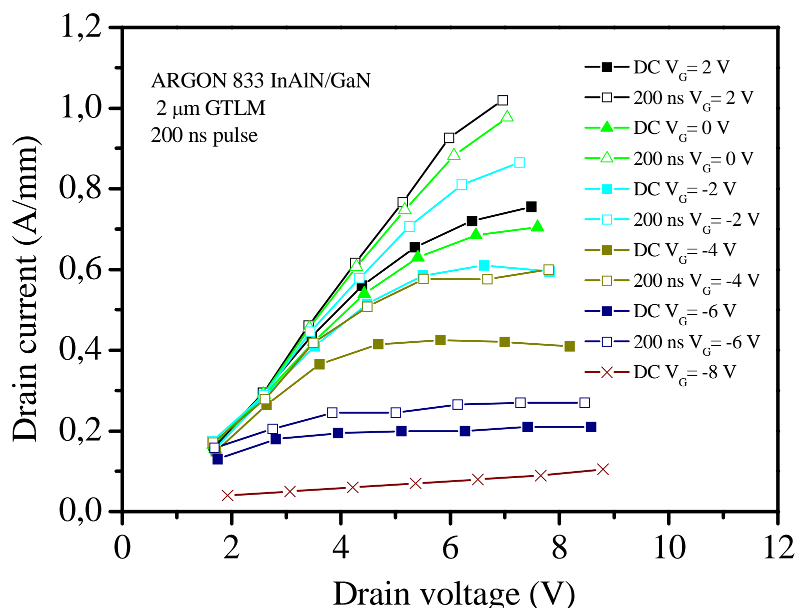

Fig. 3: DC and Gate Lag pulsed characteristics of InAlN/AlN/GaN HEMT.

I-V characterization techniques were used to determine the intensity of the electrical field at oxide breakdown which was found to be 5,5 MV/cm. 1.5 A/mm drain current at V_{GS} = 2V has been measured for 2 µm gate length MOSHEMTs (Fig. 4), and 1.4 A/mm for Schottky HEMTs (Fig. 5).

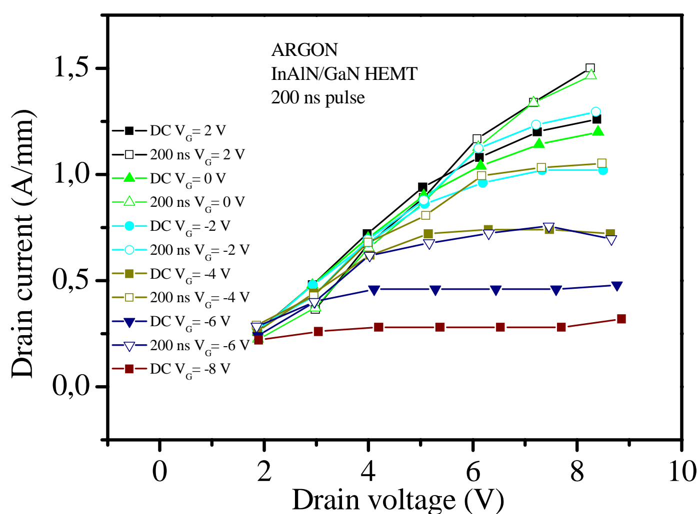

Fig. 4: I_D-V_{DS} characteristics of 2µm gate length InAlN/GaN MOSHEMT with Ar pre-treatment. V_{GS} swept from -8 to 2 V with -2 V step.

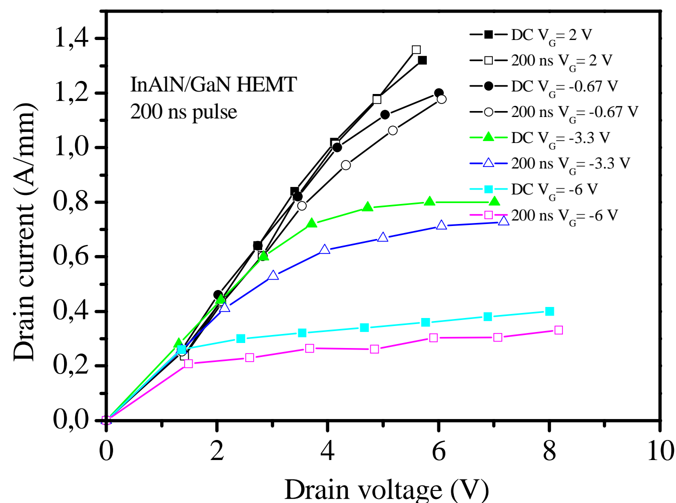

Fig. 5: I_D-V_{DS} characteristics of 2 μm gate length InAlN/GaN HEMT. V_{GS} swept from -8 to 2 V with -2 V step.

Conclusion

In conclusion we described technology and performance of InAlN/GaN MOS HEMT. We show that GaN-based MOS HEMTs (Al_2O_3/Ar) show a reduction of the gate leakage current of two orders of magnitude. For practical application point of view it is necessary to reduce this value further. The important result is that in these devices there is not gate lag effect.

Acknowledgement

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References

[1] J.Kuzmík, A. Kostopoulos, G. Konstantinidis, J.F. Carlin, A. Georgakilas, D. Pogany, “InAlN/GaN HEMTs: a first insight into technological Optimization,” *IEEE Transaction on electron devices.,* vol.53, no. 3, pp. 422-426, March 2006.