Fabrication of Narrow Split Contacts for Nanocrystal Investigations

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A simple method for producing metallic electrodes with gaps below 10 nm is presented. The fabrication of these electrodes is achieved by electron beam (e-beam) lithography and shadow evaporation. Thereby the gap width can be adjusted directly by the exposure time in the lithography process. At the moment we can create gaps as small as 4 nm. In later investigations such electrodes will be used for electrical transport studies of nanocrystals made of different materials and sizes.

Introduction

Using colloidal techniques, nanocrystals can be made of different materials [1]. The size of these nanocrystals can be easily changed via the fabrication conditions. The size is e.g. ranging from 5 to 15 nm for IV-VI semiconductors. For investigation of electrical transport properties it is necessary to have electrodes with different gap sizes fitting to the size of the nanocrystals. One way of producing them is by e-beam lithography using a scanning electron microscope (SEM) combined with shadow evaporation.

A single electron transistor can be fabricated with a nanocrystal in between two electrodes and in combination with an additional gate [2] (see Fig. 1). Such a device has the same behavior as common quantum dots produced by lithography processes [3]. In this case, the electrons tunnel one by one from the source electrode to the nanocrystal and from the nanocrystal to the drain electrode. This current is switched on and off by the applied gate voltage from the conducting p-Si substrate which is isolated with the oxide layer from the contacts.

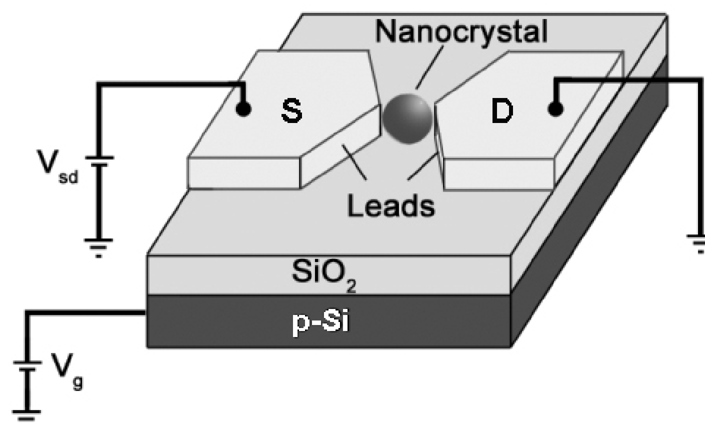

Fig. 1: Schematic picture of a nanocrystal single electron device consisting of two side contacts and an underlying conducting substrate as a plunger gate.

Experimental

The used high-doped Si substrates have a 100 nm thick SiO_2 cover layer. First they are consecutively cleaned in acetone, trichloroethylene, acetone and methanol in an ultrasonic bath for 5 minutes each. The positive photoresist Allresist AR-P 671.04 950K is spun onto the substrates at 6000 rpm for 1 minute. The photoresist is made of a solution of 4% 950K PMMA in chlorobenzene. Therewith a uniform layer with a thickness of 250 nm is achieved. The coated substrates were annealed at 160 °C for 60 minutes. Afterwards the samples are exposed with a Leo 35 scanning electron microscope. The required mask was designed with the ELPHY Plus software. In order to find the ideal mask design, different contact tip shapes were tested. We get the best results with obtuse tip shapes.

After exposure the contact electrode shape is created in the photoresist layer by putting it into a developer and a stopper for 2 minutes and 30 seconds, respectively. The samples are evaporated with an 8 nm Cr layer and a 50 nm Au layer, where the Cr layer ensures a good mechanical contact between SiO_2 and gold. In a lift-off process, the residual photoresist together with the metallic layers on top of it is removed at 75°C for 2 hours.

To apply an external voltage to the contact electrodes bonding pads are required. These pads are produced by optical lithography using the photoresist Shipley S1813 at 4000 rpm for 1 minute, baking at 90°C for 10 minutes and UV-exposure through a mask. After resist development, a 300 nm Al layer is deposited and the remaining resist is removed again. We could produce electrodes with gaps as small as 10 nm with this method.

Because of electron scattering an undercut is formed into the photoresist. Between the two electrodes the resist is so small that the undercuts are overlapping and we get a kind of bridge (Fig. 2(a)).

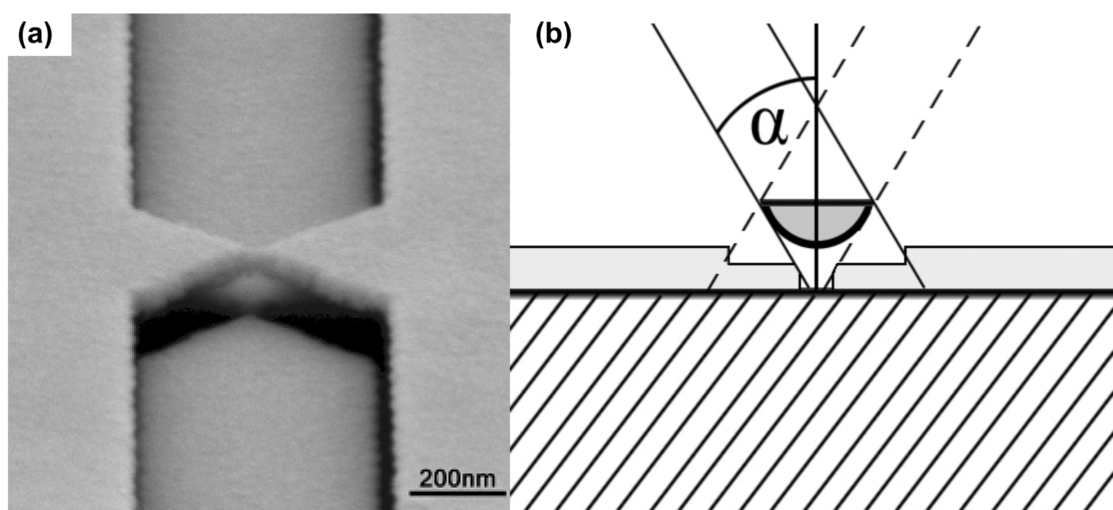

Fig. 2: (a) SEM picture of two electrodes after evaporation and before lift off; you can see the photoresist bridge covered by the Cr and Au layer; (b) schematic picture of cross section of the photoresist bridge during shadow evaporation; the first layer is deposited from right at angle of $-\alpha$, the second one is deposited from left at angle α

By using shadow evaporation we can reduce the width of the gap. For this we deposited two gold layers with a thickness of 25 nm at α = +/- 6.67° instead of one 50 nm

layer at normal incidence (Fig. 2(b)). With this technique gaps up to 4 nm are possible (Fig. 3).

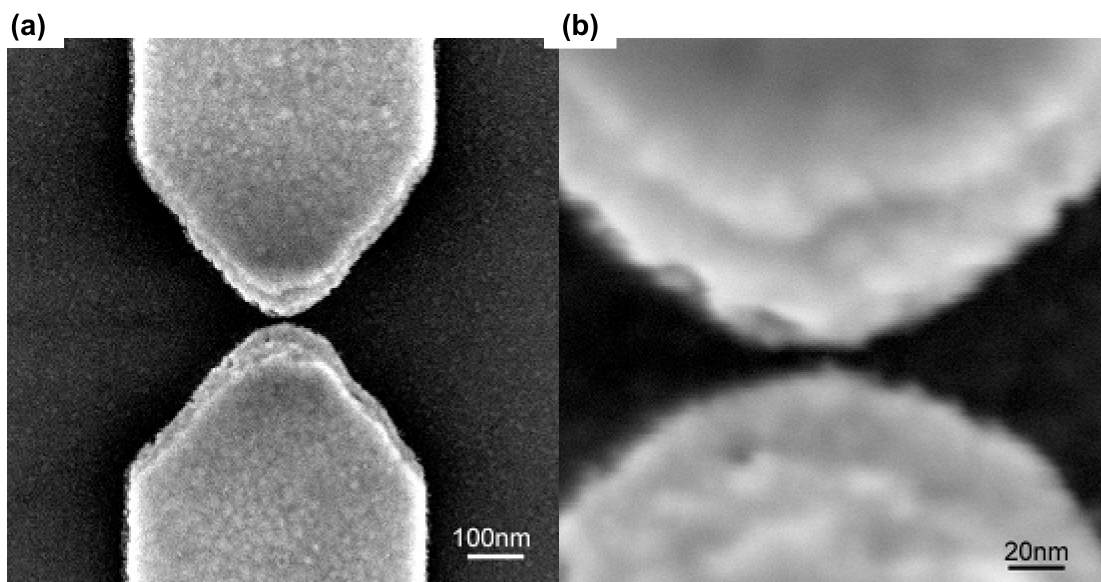

Fig. 3: SEM pictures of a pair of electrodes with different magnifications; gap width: 5.5 nm

To get the nanocrystal onto the substrate, the drop casting method is used (Fig. 4). You can see in picture Fig. 4(b), there are a lot of crystals between the electrodes. However, for general transport studies, and especially studies on the nanocrystal-SET, we just want charge transport through one single nanocrystal. However the tunneling exponential decay length is very small. A simple estimation determines this length to 1 Å. Thus, the electrons can only tunnel into well placed nanocrystals.

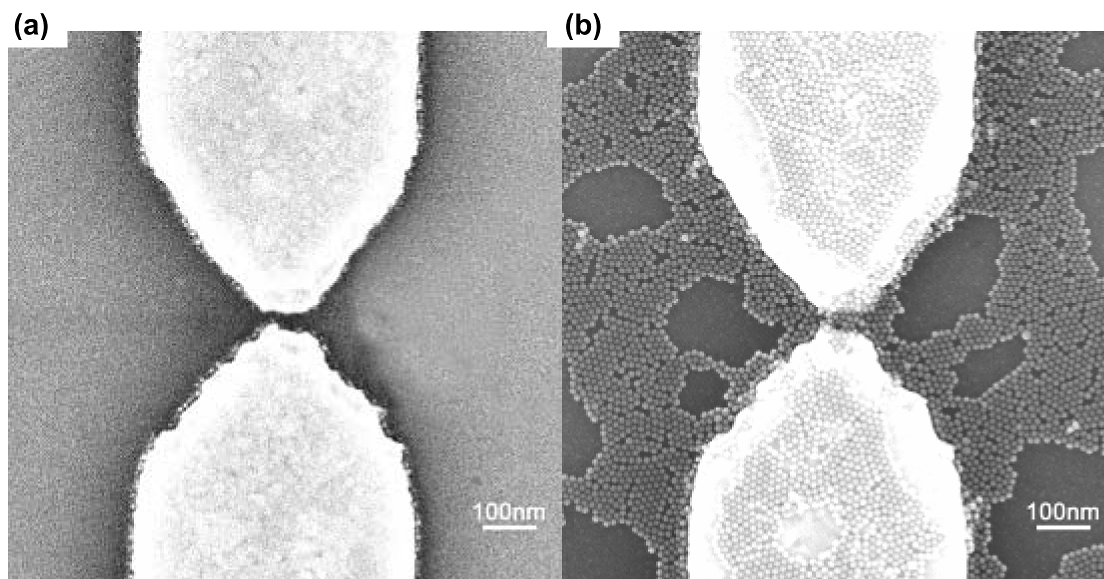

Fig. 4: SEM picture of a pair of electrodes; (a) before drop casting (b) after drop casting FeO nanocrystal (d = 12nm)

Conclusion

A simple technique has been developed to fabricate electrodes with sub-10 nm gaps. In future experiments these electrodes will be used to investigate electrical transport through nanocrystals and SET made of nanocrystals with Si substrate as back gate.

Acknowledgements

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References

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